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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/618,416	07/11/2003	Terry P. Borer	ALT.P021	7068

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EXAMINER	
SIEK, VUTHE	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 01/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/618,416	BORER ET AL.	
	Examiner	Art Unit	
	Vuthe Siek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☒ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to application 10/618,416 filed on 7/11/2003. Claims 1-33 remain pending in the application.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-33 are rejected under 35 U.S.C. 102(e) as being anticipated by Mason et al. (6,817,005).

4. As to claims 1 and 25, Mason et al. teach a method for designing a system on a target device unitizing logic devices (PLDs) (see Figs. 1-8 and its description, summary) comprising generating options for utilizing resources on the PLDs in response to user specified constraints (creating unelaborated modules, determining size, location of each unelaborated module to be implemented on PLDs corresponding to determining possible locations to place a component and move the component, user constraints); and refining the options (performing optimizations of placement and routing) for utilizing the resources on the PLDs independent of the user specified constraints (with constraints and without user constraints, see col. 9; the floorplanner tool is used to create position and range (size and shape) constraints for each module, and locate top-

level logic as well as module ports and any associated constrained, see at least see summary).

5. As to claims 12 and 19, remarks set forth in rejecting claims 1 and 25 equally apply in rejection of claims 12 and 19. Mason et al. teach that the same information is used in the placing (claim 12) by the floorplanner tool that is used by a designer to create position and range (sizes, shapes, and locations) constraints for each module and locate top-level logic as well as module ports and any associated constrained pseudo logic and routing (claim 19) stages, thereby enabling the place and route tools to perform certain optimizations (at least see summary, placing and routing description from col. 14, line 49). It is noticed that moving a component is done during placing, routing and optimizing of a circuit design. Mason et al. also teach guide file for placer and router tool (col. 22) corresponding to routing strategies.

6. As to claims 2-3, 16-17 and 26-27, Mason et al. teach refining the options for utilizing the resources is performed in response to the options not satisfying design parameters (performing optimization of modules placement and routing, modifications allowing fine-tuning of the design to meet timing constraints; at least see col. 12-14).

7. As to claims 4, 18, 24 and 28, Mason et al. teach multiple guides used in placer and router tool, where the placer and router tool iteratively steps through each one and guides the placement and routing of logic corresponding to the logic in the guide file (col. 22). Since the guide file provides complete information to perform placing and routing including optimization, the guide file must include a threshold number of options

generated/number of possible locations/number of routing strategies in order to quickly implementing a final product according to user defined constraints.

8. As to claims 5 and 29, Mason et al. also teach triggering event (col. 9, col. 13, col. 17).

9. As to claims 6 and 30, Mason et al. teach placing and routing tool used to determine locations to place components (modules, logic) within user-defined logic regions on the target device (see summary, col. 10, 14, 22).

10. As to claim 7, Mason et al. teach placing and routing tool used to determine locations to place components (modules, logic) within user-defined logic regions on the target device (see summary, col. 10, 14, 22). It is noticed that cost function is known to one skill in the art and must be used during placement, routing and optimizing a circuit design and must be used during these processes. Therefore, evaluating the locations with a cost function and accepting the locations if the cost function yields a desired value is inherently included with above design process as taught by Mason et al.

11. As to claims 8 and 31-33, Mason et al. teach a constraint editor (see summary) to generate user constraints file and create new constraints for repeating mapping, placing and routing as necessary in order to comply with design requirements (at least see summary, col. 12, 13, 14, 18, 22). This would suggest the claimed limitations of determining locations to place the components on the target device and determining routing resources to allocate to the user specified signals on the PLDs by removing constraints associated with the user-defined logic regions and the user specified routing constraints.

12. As to claims 9-10, Mason et al. teach determining routing resources to allocate to user specified signals on the target device in response to user specified routing resources (user defined constraints file, routing resources, col. 12, 14, 18, 22). Mason et al. also teach the placer and router tool iteratively steps through each one and guides the placement and routing of logic corresponding to the logic in the guide file (col. 22). Thus, the placer and router must re-select routing resources if the routing resource selection do not satisfy the user specified routing constraints in order to optimize placement and routing, to thereby minimizing area and delay.

13. As to claim 11, Mason et al. teach a constraint editor (see summary) to generate user constraints file and create new constraints for repeating mapping, placing and routing as necessary in order to comply with design requirements (col. 12, 13, 14, 18, 22). This would suggest the claimed limitations of determining locations to place the components on the target device by removing constraints associated with the user-defined logic regions.

14. As to claim 13, Mason et al. teach placing and routing tool used to determine locations to place components (modules, logic) including initial design phase, active module stage and assembly phase within user-defined logic regions on the target device (see summary, col. 10, 14, 22). Placer and router tool perform moving the user defined logic region to a new location, as Mason et al. suggest that after each guide is complete, the logic just guided will be marked so that the next guide operation will not move this logic. It is noticed that cost function is known be a metric that must be used during placing, routing and optimizing a circuit design. Therefore, the cost function must

be included during placement, routing and optimizing a circuit design as taught by Mason et al.. Therefore, evaluating a cost function associated with the user defined logic region in the new location is included within placing, routing and optimizing a circuit design process as taught by Mason et al.

15. As to claim 14, Mason et al. teach team leader uses the floorplanner tool to manually position each module (whether new, additional module, or moved module), the interface circuitry, and the global resources/signals within the target PLD. The floorplanner tool then outputs certain user constraint files "UCF" that will be used in each module's implementation. Therefore, in final implementation, after all of the modules have been published (implemented) to the team leader, the final implementation may require additional constraints not initially envisioned by the team leader (determining a timing of the system requirements in new locations), thereby affecting certain module implementations within the design. Thus, this would require re-implementation and republish their changes to the team leader. This would include requirement of routing resources associated with the user defined logic region in the new location. Thereby, after any changes have been made and the design finally meets all required criteria, the design can be implemented like any other design (see at least col. 7).

16. As to claim 15, Mason et al. initial design phase (see summary, col. 22). It is noticed that cost function is known be a metric that is used during placing, routing and optimizing a circuit design to one skill in the art. Therefore, the cost function must be used during placement, routing and optimizing a circuit design as taught by Mason et al.

Therefore, evaluating a cost function as the user defined logic region and the component are moved is included within placing, routing and optimizing a circuit design process as taught by Mason et al. in order to determine whether the component moved would optimize the user defined logic region.

17. As to claims 20-21, Mason et al. teach routing resources for user specified signal on the PLDs in response to the user specified constraints; and selecting routing resources for a non-user specified signal on the PLDs without utilizing the user specified routing constraints (see summary, col. 9, col. 11-15, 18, 22).

18. As to claims 22-23, Mason et al. teach placing and routing according to guide files and based user specified constraints and timing constraints (at least see summary, col. 22).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vuthe Siek whose telephone number is (571) 272-1906. The examiner can normally be reached on Increase Flextime.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Vuthe Siek